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Paige E. Snyder
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Nie et al.

Group Art Unit: Not Assigned

Serial No.: Not Assigned

Examiner: Not Assigned

Filed: Herewith

Docket No.: 1406/13

For: HIGH SPEED PROCESSOR

* *

PRELIMINARY AMENDMENT

Commissioner for Patents
BOX PATENT APPLICATION
Washington, D.C. 20231

Dear Sir:

Kindly amend the subject application as follows:

IN THE SPECIFICATION:

Please insert a paragraph heading on page 1 of the English translation of the subject application, before line 5, as follows:

--Technical Field --.

Please insert a paragraph heading on page 1 of the English translation of the subject application, before line 9, as follows:

--Related Art --.

Please insert a paragraph heading on page 5 of the English translation of the subject application, before line 5, as follows:

--Summary of the Invention --.

Please insert a paragraph heading on page 8 of the English translation of the subject application, before line 25, as follows:

--Detailed Description of the Invention--.

IN THE CLAIMS:

Please delete the paragraph heading "Patent Claims" on page 16 of the English translation of the subject application, and insert in place thereof the paragraph heading:

--CLAIMS--

Please insert the paragraph heading on page 16 of the English translation of the subject application, before line 3, as follows:

-- What is claimed is: --.

Please amend claims 1-16 and 19-23 as follows:

1. (Amended) A high speed processor having:

a data processing unit for processing data;

a data memory which is connected to the data processing unit via a data bus and can be addressed by the data processing unit via a data memory address bus;

at least one input interface buffer which is connected to the data bus and has the purpose of buffering input data;

at least one output interface buffer which is connected to the data bus and has the purpose of buffering output data;

the input interface buffer and the output interface buffer being directly addressable by the data processing unit via an interface address bus.

2. (Amended) The high speed processor as claimed in claim 1, wherein the data memory contains at least one RAM memory.

3. (Amended) The high speed process as claimed in claim 1, wherein the data processing unit is connected to the ROM memory which store program data.

4. (Amended) The high speed processor as claimed in claim 1, wherein the data processing unit is an RISC data processing unit.

5. (Amended) The high speed processor as claimed in claim 1, wherein the data processing unit contains a plurality of addressable internal registers.

6. (Amended) The high speed processor as claimed in claim 1, wherein the data processing unit can carry out a plurality of data transfer processor commands in order to directly exchange data between the data memory, the registers and the interface buffers.

7. (Amended) The high speed processor as claimed in claim 1, wherein when a first data transfer processor command is carried out by the data processing unit, the input data buffered in the input interface buffer is transmitted directly into an internal register for data processing.

8. (Amended) The high speed processor as claimed in claim 1, wherein when a second data transfer processor command is carried out by the data processing unit, the input data buffered in the input interface buffer is transmitted directly into an output interface buffer for the outputting of data.

9. (Amended) The high speed processor as claimed in claim 1, wherein when a third data transfer processor command is carried out by the data processing unit, the data buffered in an internal register of the data processing unit is transmitted directly into the output interface buffer for the outputting of data.

10. (Amended) The high speed processor as claimed in claim 1, wherein when a fourth data transfer processor command is carried out, the input data

buffered in an input interface buffer is transmitted directly into the data memory for storage.

11. (Amended) The high speed processor as claimed in claim 1, wherein when a fifth data transfer processor command is carried out by the data processing unit, the data stored in the data memory is transmitted directly into the output interface buffer for the outputting of data.

12. (Amended) The high speed processor as claimed in claim 1, wherein the input interface buffer is connected to an analog/digital converter.

13. (Amended) The high speed processor as claimed in claim 1, wherein the output interface buffer is connected to a D/A converter.

14. (Amended) The high speed processor as claimed in claim 1, wherein the input interface buffer and the output interface buffer are connected to the data processing unit via a control signal bus.

15. (Amended) The high speed processor as claimed in claim 1, wherein the input interface buffer is an xDSL interface buffer for buffering xDSL data.

16. (Amended) The high speed processor as claimed in claim 15, wherein the xDSL input interface buffer has a data frame detecting device for detecting a data frame synchronization data pattern.

19. (Amended) The high speed processor as claimed in claim 1, wherein the output interface buffer is a PCM interface buffer for buffering PCM data.

20. (Amended) The high speed processor as claimed in claim 1, wherein each internal register has a plurality of memory locations for different data words.

21. (Amended) The high speed processor as claimed in claim 1, wherein each processor task executed by the data processing unit is assigned a separate internal register.

22. (Amended) The high speed processor as claimed in claim 1, wherein peripherals can be connected to the interface buffers.

23. (Amended) The high speed processor as claimed in claim 1, wherein the input interface buffer and the output interface buffer can be configured.

REMARKS

The amendments to the specification as set forth above are intended to clarify and set apart the various sections of the subject application.

The amendments to the claims as set forth above are intended to remove all multiple dependent claims from the subject application and to more particularly point out and distinctly claim the subject matter of the invention.

Attached hereto is a marked-up version of the specification and claims 1-16 and 19-23, which illustrates all of the changes made to the specification and claims pursuant to 37 CFR §1.121. The attached page is captioned "**Version With Markings To Show Changes Made**". Deleted language is bracketed and added language is underlined.

The Commissioner is hereby authorized to charge any deficiencies or credit any overpayments in connection with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

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1406/13 REJ/lsg

Serial No.: Not yet assigned

Version With Markings To Show Changes Made

IN THE SPECIFICATION:

The paragraph heading has been inserted on page 1 of the English translation of the subject application, before line 5, as follows:

Technical Field

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Summary of the Invention

The paragraph heading has been inserted on page 8 of the English translation of the subject application, before line 25, as follows:

Detailed Description of the Invention

IN THE CLAIMS:

The paragraph heading "Patent Claims" has been deleted and the paragraph heading has been inserted in place thereof on page 16 of the English translation of the subject application, as follows:

CLAIMS

The paragraph heading has been inserted on page 16 of the English translation of the subject application, before claim 3, as follows:

What is claimed is:

1. (Amended) A high speed processor having:

a data processing unit [(13)] for processing data;

a data memory [(20)] which is connected to the data processing unit via a data bus [(10)] and can be addressed by the data processing unit [(13)] via a data memory address bus [(18)];

at least one input interface buffer [(9)] which is connected to the data bus [(10)] and has the purpose of buffering input data;

at least one output interface buffer [(26)] which is connected to the data bus [(10)] and has the purpose of buffering output data;

the input interface buffer [(9)] and the output interface buffer [(26)] being directly addressable by the data processing unit [(13)] via an interface address bus [(24)].

2. (Amended) The high speed processor as claimed in claim 1, wherein the data memory [(20)] contains at least one RAM memory [(19)].

3. (Amended) The high speed process as claimed in claim 1 [or 2], wherein the data processing unit [(13)] is connected to the ROM memory [(15)] which stores program data.

4. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the data processing unit [(13)] is an RISC data processing unit.

5. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the data processing unit [(13)] contains a plurality of addressable internal registers.

6. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the data processing unit [(13)] can carry out a plurality of data transfer processor commands in order to directly exchange data between the data memory [(20)], the registers [(14)] and the interface buffers [(9, 26)].

7. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein when a first data transfer processor command is carried out by the data processing unit [(13)], the input data buffered in the input interface buffer [(9)] is transmitted directly into an internal register [(14)] for data processing.

8. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein when a second data transfer processor command is carried out by the data processing unit [(13)], the input data buffered in the input interface buffer is transmitted directly into an output interface buffer [(26)] for the outputting of data.

9. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein when a third data transfer processor command is carried out by the data processing unit [(13)], the data buffered in an internal register [(14)] of the data processing unit [(13)] is transmitted directly into the output interface buffer [(26)] for the outputting of data.

10. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein when a fourth data transfer processor command is carried out, the input data buffered in an input interface buffer [(9)] is transmitted directly into the data memory [(20)] for storage.

11. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein when a fifth data transfer processor command is carried out by the data processing unit [(13)], the data stored in the data memory [(20)] is transmitted directly into the output interface buffer [(26)] for the outputting of data.

12. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the input interface buffer [(9)] is connected to an analog/digital converter [(5)].

13. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the output interface buffer [(26)] is connected to a D/A converter [(32)].

14. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the input interface buffer [(9)] and the output interface buffer [(26)] are connected to the data processing unit [(13)] via a control signal bus.

15. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the input interface buffer [(9)] is an xDSL interface buffer for buffering xDSL data.

16. (Amended) The high speed processor as claimed in claim 15, wherein the xDSL input interface buffer [(9)] has a data frame detecting device for detecting a data frame synchronization data pattern.

19. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the output interface buffer [(26)] is a PCM interface buffer for buffering PCM data.

20. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein each internal register [(14)] has a plurality of memory locations for different data words.

21. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein each processor task executed by the data processing unit [(13)] is assigned a separate internal register.

22. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein peripherals can be connected to the interface buffers [(9, 26)].

23. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the input interface buffer [(9)] and the output interface buffer [(26)] can be configured.